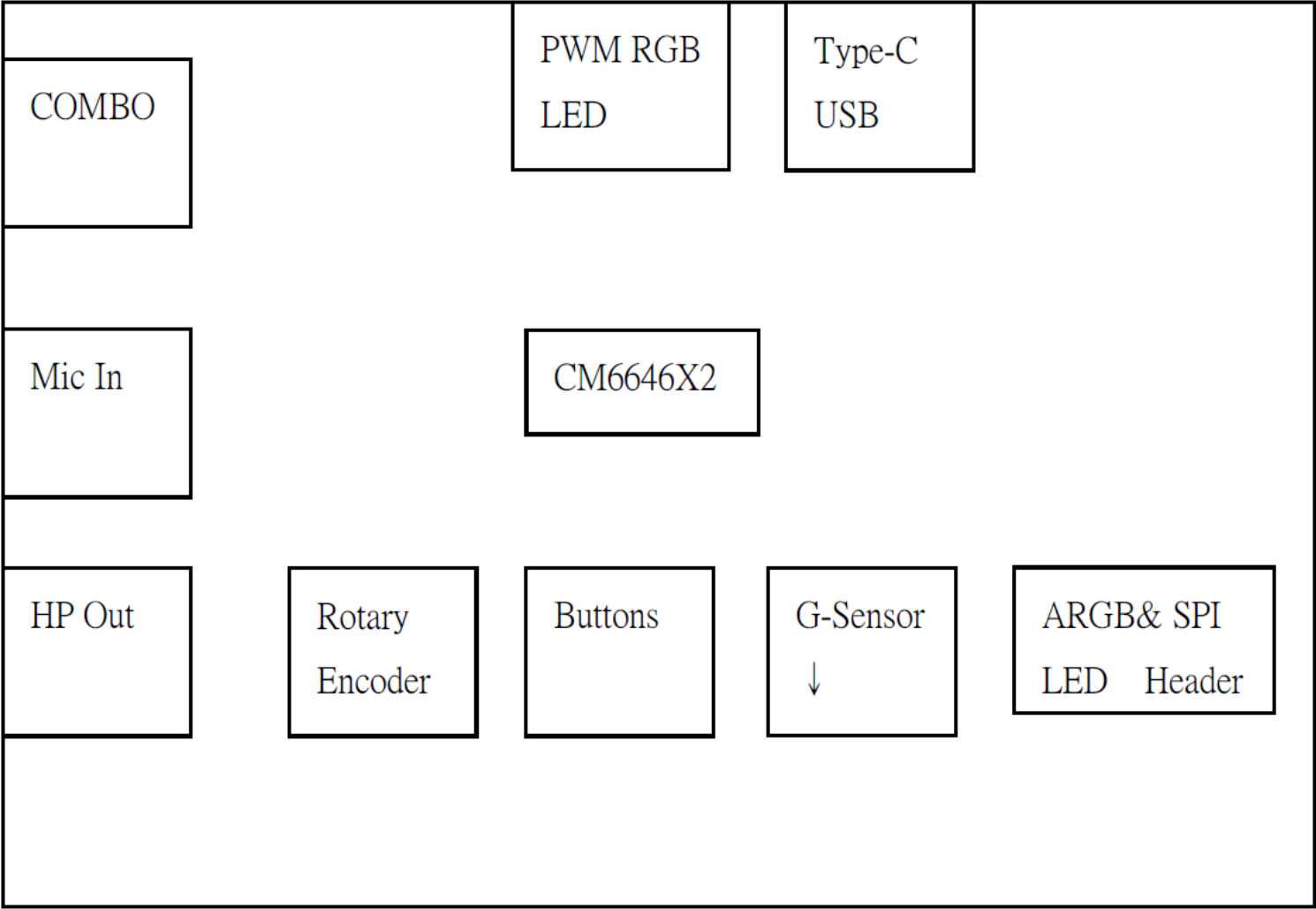
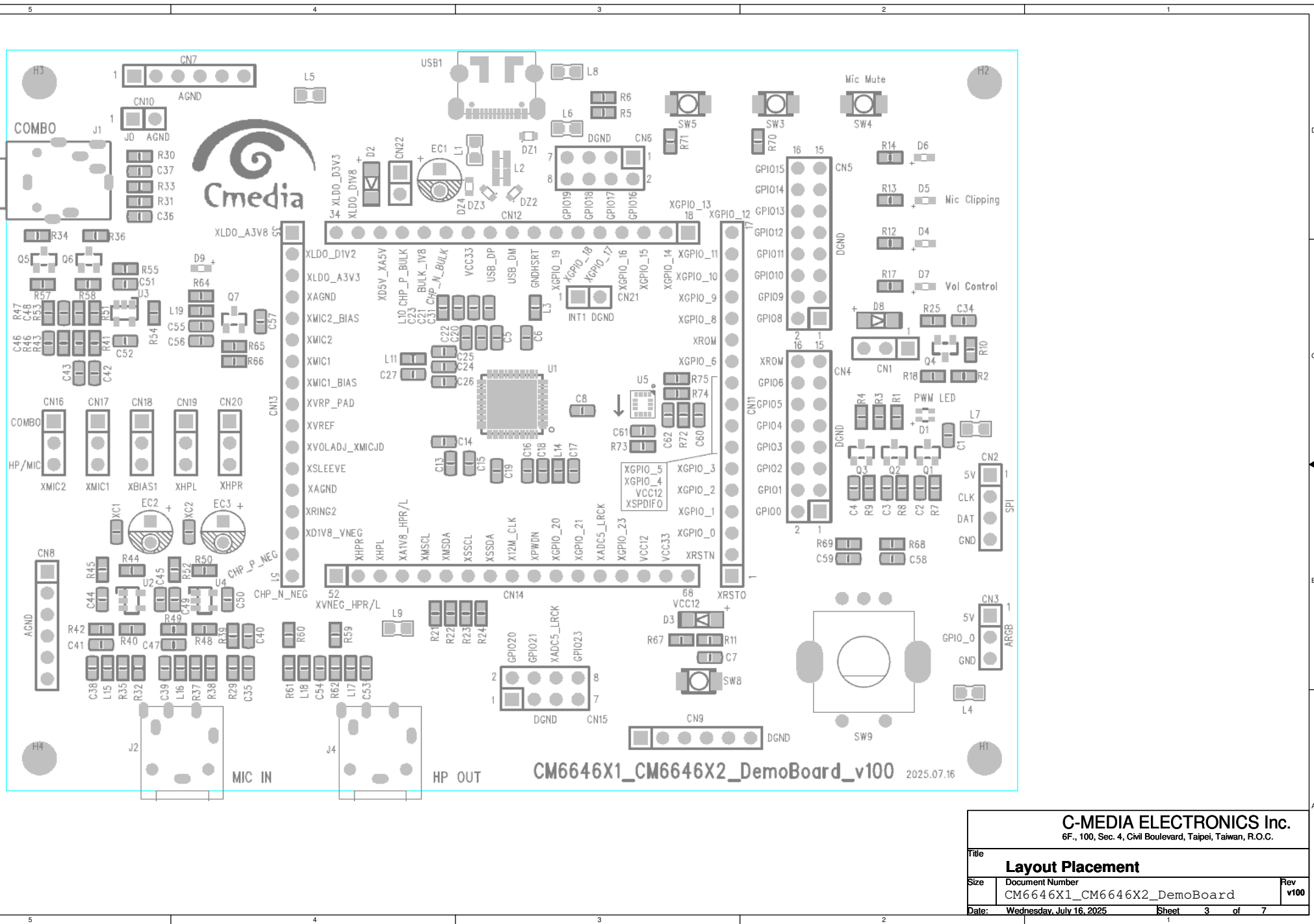


Date	Rev.	Notice	Create by
2025/04/14		NEW CREATE (CM6646X2) .	Daniel Lee
2025/07/16	v100	1.CM6646X1 and CM6646X2 are share the circuit. 2. Volume control GPIO 9,10. 3. SPI LED GPIO 0,1 ; ARGB GPIO 0. 4. Add ARGB/SPI LED 5V. 5. JD add Pull low header. 6. PWM LED to USB5V/GND_EARTH.	Daniel Lee

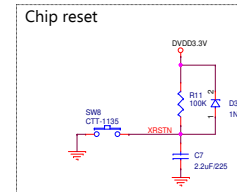
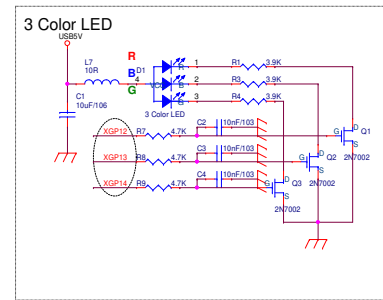
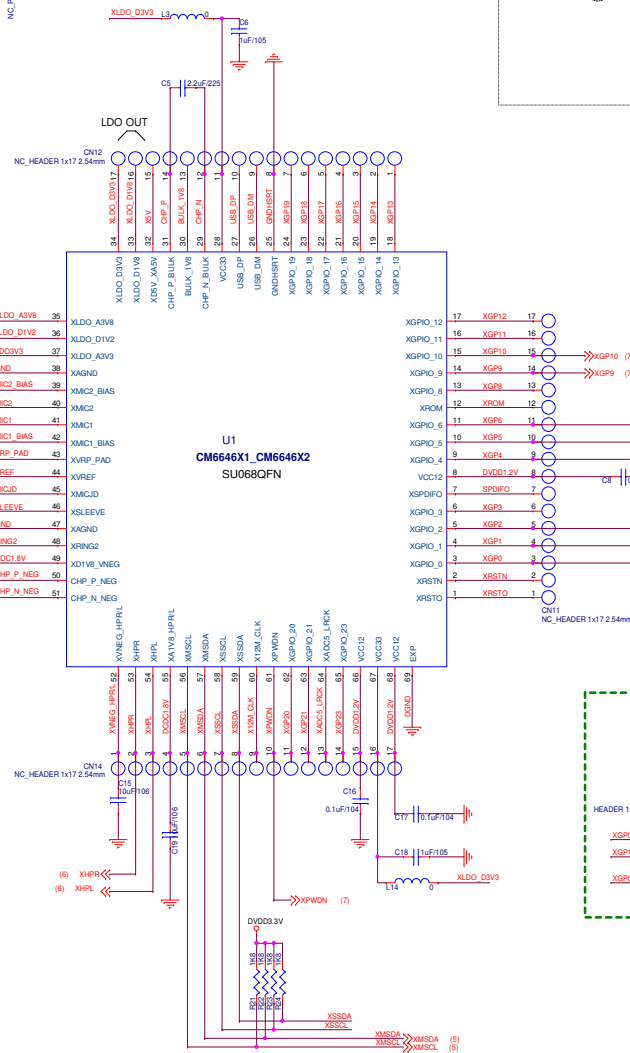
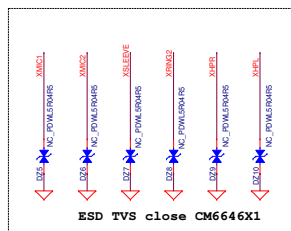
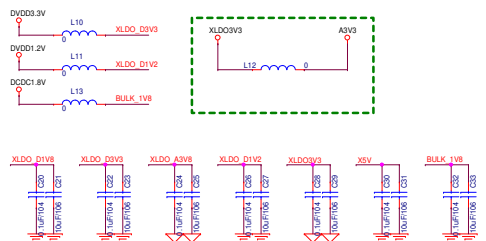
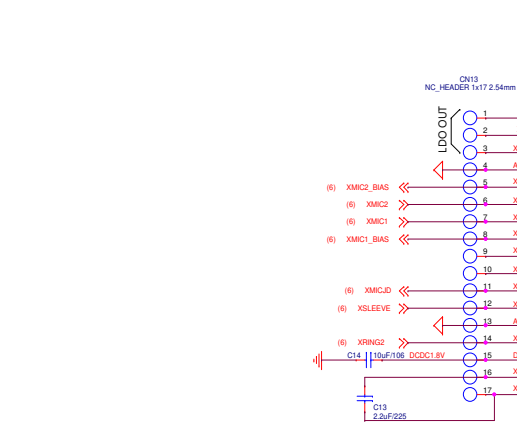
C-MEDIA ELECTRONICS Inc. 6F., 100, Sec. 4, Civil Boulevard, Taipei, Taiwan, R.O.C.			
Title			
HISTORY NOTE			
Size	Document Number		Rev v100
Date:	Wednesday, July 16, 2025	Sheet 1 of 7	



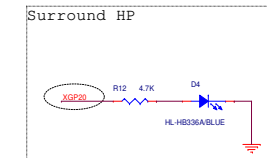


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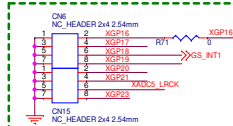
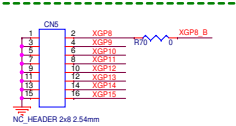
Title			
Layout Placement			
Size	Document Number	Rev	
	CM6646X1_CM6646X2_DemoBoard	v100	
Date:	Wednesday, July 16, 2025	Sheet	3 of 7

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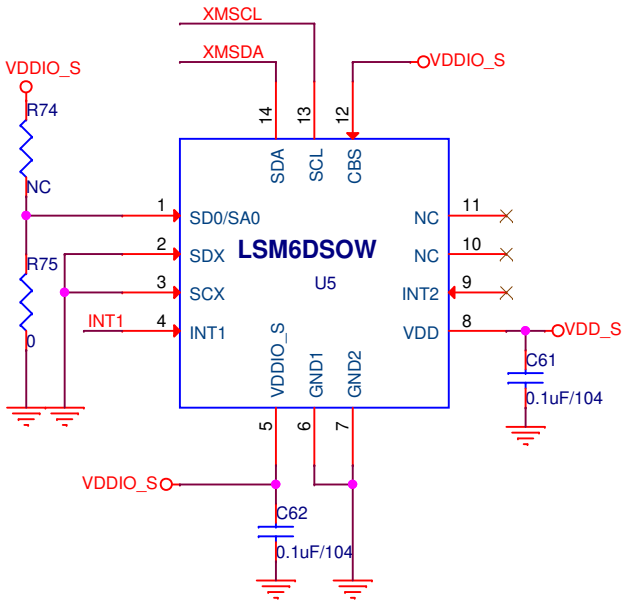
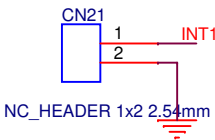
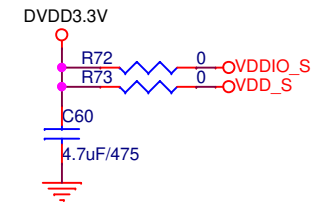
The schematic diagram illustrates the MIC Mute control circuit. A 3.3V supply is connected to a 2k resistor (R2) and a 2k3 resistor (R3). The circuit includes five switches: SW3, SW4, SW5, SW1, and NC. SW3 is labeled XGP6_B, SW4 is labeled XGP3, SW5 is labeled XGP16_B, and SW1 is labeled undefined. A pull-up resistor R10 (NC_0) is connected to the common terminal of the switches and to ground.



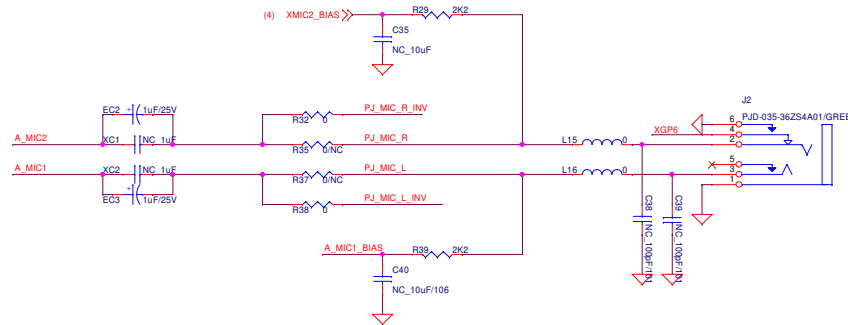
The diagram shows a red LED (D7, HL-HB336A/BLUE) connected to a 4.7K resistor (R17). A red wire, labeled XGP23, is connected to the circuit. The LED is connected to ground.



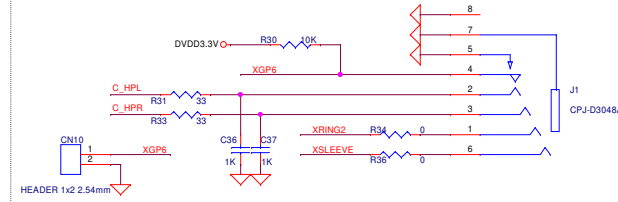
G-Sensor



3-Ring Stereo Microphone Input



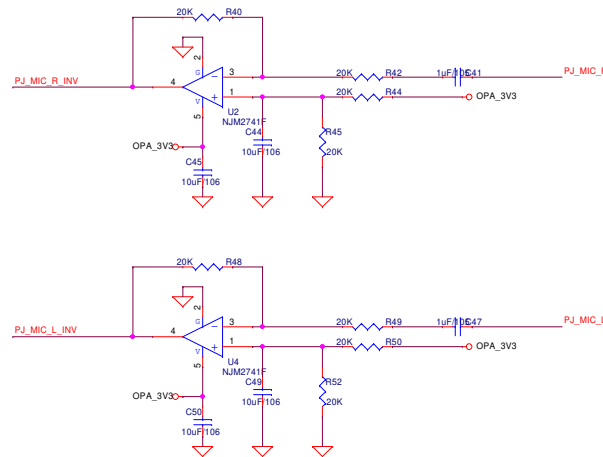
COMBO JACK



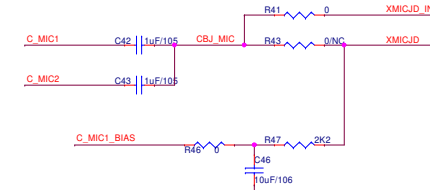
"XMICJD" is an output signal from OMTP/CTIA detection circuit

For COMBO JACK (J1) application:
C44,C46 was used for stereo recording (CBJ_MIC copy to C_MIC1 & XMIC2)

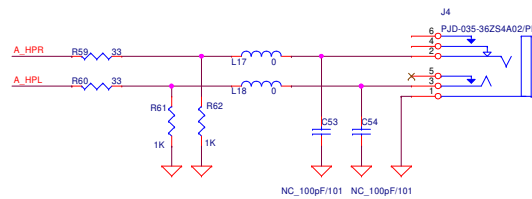
3-Ring stereo microphone inverter



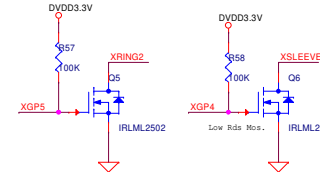
Combo jack microphone inverter



Headphone Output

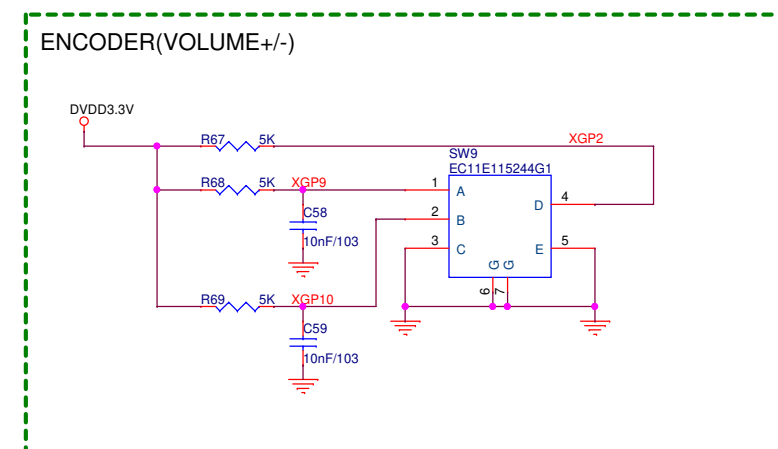
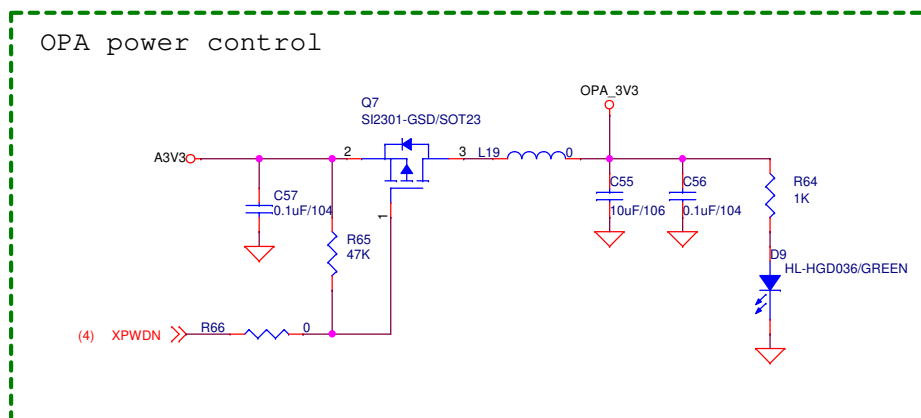


Improve Headphone crosstalk performance



- (4) XMICJD >>> XMICJD
- (4) XSLEEVE <<< XSLEEVE
- (4) XRING2 <<< XRING2
- (4) XGP6 >>> XGP6
- (4) XGP5 >>> XGP5
- (4) XGP4 >>> XGP4
- (4) XMIC2 >>> XMIC2
- (4) XMIC1 >>> XMIC1
- (4) XMIC1_BIAS >>> XMIC1_BIAS
- (4) XHPL <<< XHPL
- (4) XHPR <<< XHPR

- CN16 HEADER 1x3 2.54mm
 - 1 C_MIC2
 - 2 XMIC2
 - 3 A_MIC2
- CN17 HEADER 1x3 2.54mm
 - 1 C_MIC1
 - 2 XMIC1
 - 3 A_MIC1
- CN18 HEADER 1x3 2.54mm
 - 1 C_MIC1_BIAS
 - 2 XMIC1_BIAS
 - 3 A_MIC1_BIAS
- CN19 HEADER 1x3 2.54mm
 - 1 C_HPL
 - 2 XHPL
 - 3 A_HPL
- CN20 HEADER 1x3 2.54mm
 - 1 C_HPR
 - 2 XHPR
 - 3 A_HPR



XGPIO_9 & 10: Volume control (順時鐘旋轉)
HP vol. up / CSPK Vol. down (Banlance volume mode) ; CMA112 playback volume up (Master volume mode)

XGPIO_9 & 10: Volume control (逆時鐘旋轉)
HP vol. down / CSPK Vol. up (Banlance mode) ; CMA112 playback volume down (Master volume mode)

XGPIO_2:Volume control switch
Banlance (Default) / Master volume mode switch

(4) XGP9 << XGP9
(4) XGP10 << XGP10
(4) XGP2 << XGP2